

## CLAIMS

What is claimed is:

- 1     1.     A method of designing an integrated circuit comprising programming a processing path  
2     within the integrated circuit according to a first substitute circuit comprising substitute inputs and  
3     a substitute output, wherein a truth table representing the first substitute circuit is identical to a  
4     truth table representing a first sequence of Boolean elements representing a processing path, and  
5     wherein the first substitute circuit is not definable by a sequence of basic Boolean circuits.
  
- 1     2.     The method according to claim 1 further comprising generating the first substitute circuit.
  
- 1     3.     The method according to claim 2 further comprising receiving the first sequence of basic  
2     Boolean elements.
  
- 1     4.     The method according to claim 1 wherein the processing path further comprises a flip  
2     flop at a processing path input.
  
- 1     5.     The method according to claim 2 further comprising the step of reducing the first  
2     sequence of Boolean elements into at least one intermediate equivalent circuit prior to the step of  
3     generating a first substitute circuit.
  
- 1     6.     The method according to claim 2 wherein the integrated circuit is a MOS circuit.
  
- 1     7.     The method according to claim 3 wherein the first sequence of basic Boolean elements is  
2     less than or equal to twenty Boolean operators.

1     8.     The method according to claim 3 wherein the first sequence of basic Boolean elements  
2     comprises a logical sequence greater than twenty Boolean elements.

1     9.     The method according to claim 3 wherein the step of receiving the first sequence of basic  
2     Boolean elements precedes the step of generating a first substitute circuit.

1     10.    The method according to claim 1 wherein the step of programming is preceded by the  
2     steps:

- 3         a.     generating a plurality of sequences of basic Boolean elements respectively defined
- 4             by a plurality of truth tables;
- 5         b.     generating a respective plurality of substitute circuits not definable by a sequence
- 6             of basic Boolean elements, including the first substitute circuit, wherein a
- 7             sequence of basic Boolean elements and its respective substitute circuit are
- 8             defined by a same truth table;
- 9         c.     storing the plurality of sequences of basic Boolean elements in a library; and
- 10        d.     storing the plurality of substitute circuits in the library in a relationship
- 11             corresponding to their respective sequence of basic Boolean elements.

1     11.    The method according to claim 10 further comprising the steps:

- 2         e.     receiving a first sequence of basic Boolean elements; and
- 3         f.     searching the library for the first substitute circuit.

1     12.    The method according to claim 11 further comprising the steps:

- 2         a.     failing to locate the first sequence of basic Boolean elements within the library;
- 3         b.     generating the first substitute circuit; and
- 4         c.     adding the first substitute circuit to the library.

1     13.     The method according to claim 11 wherein the step of receiving the first sequence of  
2     basic Boolean elements is followed by the steps:

- 3             a.     locating the first sequence of Boolean elements within the library; and  
4             b.     locating the first substitute circuit within the library corresponding to the first  
5             sequence of Boolean elements.

1     14.     The method according to claim 10 wherein the library comprises a digital memory.

1     15.     The method according to claim 11 comprising a search engine for searching the library  
2     for the first sequence of basic Boolean elements.

1     16.     An apparatus for reducing a throughput time of a processing path of basic logic elements  
2     within an integrated circuit, the apparatus comprising a programming module for programming a  
3     first substitute circuit into the processing path of the integrated circuit, wherein the substitute  
4     circuit is not defined by a sequence of basic Boolean circuits, and wherein the substitute circuit is  
5     defined by a truth table identical to a truth table defining a processing path comprised of basic  
6     Boolean circuits.

1     17.     The apparatus according to claim 16 wherein the processing path comprises an input flip  
2     flop.

1     18.     The apparatus according to claim 16 wherein the integrated circuit is an MOS circuit.

1     19.     The apparatus according to claim 16 further comprising a circuit generation module  
2     configured to analyze a sequence of basic Boolean elements and generate a complimentary  
3     substitute circuit.

1     20.   The apparatus according to claim 19 further comprising a reduction module configured to  
2     reduce a first sequence of Boolean elements into an intermediate circuit sequence.

1     21.   The apparatus according to claim 16 further comprising:

- 2           a.     a sequence generator for generating a plurality of sequences of Boolean elements,  
3                 wherein the circuit generation module is configured to generate a complimentary  
4                 substitute circuit for each sequence of Boolean elements generated;  
5           b.     a library for storing the plurality of sequences of Boolean elements such that each  
6                 Boolean element is stored in a correlation to its complimentary substitute circuit;  
7           c.     a search module for searching the library for a first sequence of Boolean elements;  
8                 and  
9           d.     a retrieval module for retrieving a substitute circuit from the library.

1     22.   The apparatus according to claim 21 wherein the library is stored on a digital medium.

1     23.   A method of programming a processing path comprising an input flip flop in a MOS  
2     integrated circuit comprises:

- 3           a.     receiving a first sequence of basic Boolean elements;  
4           b.     reducing the first sequence of basic Boolean elements to an equivalent sequence  
5                 of elements;  
6           c.     generating a substitute circuit from the equivalent sequence of elements; and  
7           d.     programming a processing path in the MOS integrated circuit according to the  
8                 substitute circuit, wherein the substitute circuit is not definable by a sequence of  
9                 basic Boolean elements, and wherein the substitute circuit is generated to define a  
10                truth table that also defines the first sequence of Boolean elements.